mN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,312	06/24/2003	Kenneth W. Marr	303.859US1	8022

21186 7590 07/30/2007

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
07/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,312	MARR, KENNETH W.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-16,48-65 and 76-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16,48-65 and 76-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered October 03, 2006.

- Claims 13-16, 48-65 and 76-78 are pending.
- Claims 13, 48, 58-59, 61, 63, 65 and 78 have been amended.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 13 recites the limitation "the first supply node" in lines 3-4 whereas the claim also recites a supply node and the supply node. It is not clear which node the Applicant is referring to.

As per claims 14-16:

These claims are rejected by virtue of their dependency.

Response to Amendment

Applicant's arguments and amendments with respect to claims 13-16, 48-65 and 76-78 filed May 21, 2007 have been fully considered but they are not persuasive.

Applicant contends that prior art of record Namekawa US Pat no. 6,115,301 does not teach: a plurality of memory segments connected in parallel with each other between the first supply node and a plurality of internal nodes, the switching units to be connected in series with one of the memory segments between the second supply node and one of

the internal nodes, each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal, a first storage node and a second storage node, and a supply control circuit. Examiner respectfully disagrees.

Firstly, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. There is no mention of how the prior art of record is distinguished from the claimed limitations. Applicant merely states that Namekawa does not teach all the limitations.

Examiner would like to request Applicant to consider "Furthermore, the present invention provides a semiconductor memory device comprising: a memory cell array in which a plurality of memory cells are arranged; a redundant memory cell array arranged to be adjacent to one end of the memory cell array; a plurality of data lines, connected to the memory cell array, for transferring data; a redundant data line, connected to the redundant memory cell array, for transferring data; a plurality of input/output data lines arranged in correspondence with the plurality of data lines; a first selection circuit group having a plurality of selection circuits, the selection circuits connecting the data lines to the corresponding input/output data lines; a second selection circuit group having selection circuits whose number is equal to the number of selection circuits of the first selection circuit group, the selection circuits of the second selection circuit group connecting the data lines except for a data line located at the other end of the memory cell array, the

redundant data line, and the input/output data line to each other; a defective address memory circuit for storing an address of a defective data line; and a decoder group having a plurality of decode circuits, the decode circuits being arranged in correspondence with the selection circuits constituting the first and second selection circuit groups, and simultaneously turning off the selection circuit of the first selection circuit group located between the defective data line and the redundant data line and simultaneously turning on the selection circuit of the second selection circuit group." (column 4, lines 25-50).

Examiner would further like to respectfully request Applicant to consider "The switches constituting the first and second switch circuit groups 50 and 60 are controlled by the decode circuits D0, . . . , D15 constituting a decoder group 70, respectively. More specifically, the non-inverted output terminal of the decode circuit D0 is connected to the switch SW20, and the inverted output terminal is connected to the switch SW10. The non-inverted output terminal of the decode circuit D1 is connected to the switch SW21, and the inverted output terminal is connected to the switch SW11. In the same manner as described above, the non-inverted output terminal of the decode circuit D15 is connected to the switch SW215, and the inverted output terminal is connected to the switch SW115. The output terminal of a defective address memory circuit 80 is connected to the input terminals of the decode circuits D0, . . . , D15. The defective address memory circuit 80 stores the address of a defective data line, and stores data representing whether the data line is replaced. The defective address memory circuit 80 outputs, depending on an input column or row address, the address of a defective data line constituted by a signal of a plurality of bits and a signal representing whether a data line is replaced. The decode

circuits D0, . . . , D15 generally turn on the respective switches of the first switch circuit group 50 depending on an output signal from the defective address memory circuit 80, and turn off the switches of the second switch circuit group 60. On the other hand, when data lines are to be replaced, depending on an output an output signal from the defective address memory circuit 80, output signals from decode circuits corresponding to a defective data line and a redundant data line and an output signal from a decode circuit located between these decode circuits are inverted. For example, the data line DL4 has a defect, output signals from the decode circuits D0, . . . , D4 are simultaneously inverted depending on the output signal from the defective address memory circuit 80. The switches SW10, . .

, SW14 of the first switch circuit group 50 are turned off, and the switches SW20, . . . , SW24 of the second switch circuit group 60 are turned on. For this reason, the data line DL4 is replaced with the data line DL3, and the data line DL3 is replaced with the data line DL2. In the same manner as described above, the data line DL0 is replaced with the redundant data line RDL. The replacing operations by the switches are simultaneously performed depending on the output signals from the decode circuits D0, . . . , D4." (Figure 1, column 6, lines 5-55).

First and foremost Examiner would like to cite the definition of Node from Wikipedia.org; "a region in an electrical circuit where there is no change in potential."

It is clear from Figure 1 that the switches are connected in series with the memory segments with respect to the internal nodes in the memory cell array and the second supply nodes, which are the switches as in order for a switch to be working there needs to

be node to supply voltage. When the defective address memory (Figure 1 # 80) sends a select signal to the Decoders, they turn the respective switch off to electrically disconnect the memory cell array from the respective supply node (switch). The respective decoders act as a supply control circuit by isolating the memory segment using the switches. Further, the illustration of the memory cell is merely an example, however even if we incorporate that all the memory cells are exactly as depicted in Figure 1, Namekawa still reads on a first storage node and a second storage node, because every memory cell has multiple nodes if the definition is incorporated from Wikipedia.

As per the claims 76-78 Namekawa suggests that "The present invention relates to a semiconductor memory device having a defect relieving system which is applied to, e.g., a dynamic random access memory (to be referred to as a DRAM hereinafter), in particular....Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein."

The primary purpose of Namekawa's invention is to incorporate a defect relieving system in a semiconductor memory device and the DRAM is just given by example, this contention is supported by the claims, where Namekawa has cited a semiconductor memory device and not merely a DRAM. Therefore, a SRAM is also incorporated in Namekawa's teachings.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13-16, 48-65 & 76-78 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Namekawa US Pat no. 6,115,301.

As per claims 13:

Namekawa substantially teaches a device comprising: a first supply node and a second supply node (column 7, lines 3-20); a plurality of memory segments connected in parallel with each other (Figure 1 # 10); a plurality of switching units, each of the switching units connecting in series with one of the memory segments between the second supply node and one of the internal nodes (column 3, lines 23-50), wherein each of the switching units includes an input node for receiving a select signal to electrically disconnect one of the memory segments from the second supply node based on a state of the select signal (Figure 1 # 70, column 6, lines 5-30); and a redundant array for replacing at least one memory segment of the plurality of memory segments (Figure 1 # 20).

Namekawa discloses the claimed invention except for the exact location of the switching units. It would have been obvious to one having ordinary skill in the art at the

time the invention was made to place the switching units between the second supply nodes and one of the internal nodes, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 14:

Namekawa teaches the device as rejected in claim 13 above, further comprising a redundancy controller connected to the switching units for selectively setting the state of the select signal based on a number of programming signals (column 4, lines 25-50).

As per claim 15:

Namekawa teaches the device as rejected in claim 14 above, further comprising a programming unit for generating the programming signals based on a programmed address stored in the programming unit (column 7, lines 20-40).

As per claim 16:

Namekawa teaches the device as rejected in claim 13 above, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least one of the memory groups of at least one of the memory segments is defective (Figure 1 # 10).

As per claim 48:

Namekawa substantially teaches a device comprising: a first supply node and a second supply node (column 7, lines 3-20); a plurality of memory segments, each of the memory segments including a plurality of memory cells (Figure 1 # 10), each of the memory cells including: a first storage node and a second storage node (Figure 2 # 80); a latch connected to the first and second storage node and connected in between a first

internal node and a second internal node (column 1, lines 5-40); a first access element for accessing the first storage node; and a second access element for accessing the second storage node column 6, lines 25-50); a plurality of first switching units, each of the first switching units connecting in between the first supply node and one of the memory segments (column 3, lines 23-50); and a plurality of second switching units, each of the second switching units connecting between the second supply node and one of the memory segments (Figure 1 # 70, column 6, lines 5-30).

Namekawa discloses the claimed invention except for the exact location of the switching units. It would have been obvious to one having ordinary skill in the art at the time the invention was made to place the switching units between the second supply nods and one of the internal nodes, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse,* 86 USPQ 70.

As per claim 49:

Namekawa teaches the device as rejected in claim 48 above, wherein at least one of the memory segments is defective (column 3, lines 25-50).

As per claim 50:

Namekawa teaches the device as rejected in claim 48 above, wherein at least one of the memory segments has a circuit short between the first and second internal nodes (column 4, lines 30-50).

As per claim 51:

Namekawa teaches the device as rejected in claim 48 above, wherein each of the memory segments includes memory cells arranged memory cell groups, wherein at least

one of the memory groups of at least one of the memory segments is defective (Figure 1 # 10).

As per claim 52:

Namekawa teaches the device as rejected in claim 48 above, wherein in each of the memory segments, the plurality of memory cells are arranged in a plurality of rows connected in parallel between one of the first switching unit and one of the second switching units (Figure 1 # 40).

As per claim 53:

Namekawa teaches the device as rejected in claim 48 above, wherein each of the first switching units includes a transistor having a source and a drain connected between the first supply node and one of the memory segments (column 5, lines 37-50).

As per claim 54:

Namekawa teaches the device as rejected in claim 48 above, wherein each of the second switching units includes a transistor having a source and a drain connected between the second supply node and one of the memory segments (column 5, lines 37-50).

As per claim 55:

Namekawa teaches the device as rejected in claim 48 above, wherein the latch includes: a first inverter having an input node connected to the first storage node and an output node connected to the second storage node; and a second inverter having an input node connected to the second storage node and an output node connected to the first storage node (column 8, lines 25-40).

As per claims 56:

Namekawa teaches the device as rejected in claim 55 above, wherein one of the first and second access elements includes a transistor having a source and a drain connected between one of the first and second storage nodes and a bit line (column 5, lines 37-50).

As per claim 57:

Namekawa teaches the device as rejected in claim 56 above, herein the latch includes: a first pair of transistors having a common drain connected to the first storage node and a common gate connected to the second storage node; and a second pair of transistors having a common drain connected to the second storage node and a common gate connected to the first storage node (column 5, lines 37-50).

As per claims 76-78:

See Response to Amendment above.

As per claims 58-62:

Claims 58-62 are directed to a system of claims 13-16 & 48-57. Namekawa teaches as stated above, the device as set forth in claims 13-16 & 48-57. Therefore, Namekawa also teaches, as stated above, the system as set forth in claims 58-62.

As per claims 63-65:

Claims 63-65 are directed to a method of claims 13-16 & 48-57. Namekawa teaches as stated above, the device as set forth in claims 13-16 & 48-57. Therefore, Namekawa also teaches, as stated above, the method as set forth in claims 63-65.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
07/16/2007

GUY LAMARRE
PRIMARY EXAMINER